REMARKS

Paragraphs **[0005]** and **[0023]** have been amended to correct minor editorial problems. Paragraph **[0033]** has been amended to note reference designator 29, which has been added to FIGS. 1C-1E and 2.

The Final Office Action mailed October 16, 2003, has been received and reviewed. Claims 1 through 4, 6, and 11 through 29 are currently pending in the application. Claims 1 through 4, 6, 11 through 18, and 21 through 24 stand rejected. Claims 19, 20 and 25 through 29 are withdrawn from consideration as being drawn to a non-elected invention. Claims 19, 20 and 26 through 29 have been cancelled, and Applicants propose to amend claim 1 to correct a minor spelling error. Applicants respectfully request reconsideration of the application as proposed to be amended herein.

Drawings

Applicants submit herewith proposed changes to FIGS. 1C-1E and 2. Specifically, FIGS. 1C-1E have been amended to include broken lines designating depressions 29 and reference designators have been added to FIGS. 1C-1E and 2 to point out these features. Applicants submit that these changes are supported by the as-filed specification and do not introduce any new matter. Applicants respectfully request approval of the corrections to the drawings.

35 U.S.C. § 112 Claim Rejections

Claims 1 through 4, 6, 11 through 18, and 21 through 24 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention, and as failing to comply with the enablement requirements. Applicants respectfully traverse this rejection, as hereinafter set forth.

In rejecting claims 1 through 4, 6, 11 through 18, and 21 through 24, the Office asserts that the specification lacks support for the claim 1 limitation of "forming a layer of encapsulant material over substantially all of said active surface and into said channels such that a surface of

Nevertheless, in order to eliminate any confusion, Applicants have amended FIGS. 1C-1E to include broken lines designating the depressions already shown in FIG. 2 and described in the specification, and have added the reference designator "29" to clearly point out these features. Accordingly, Applicants respectfully request that the rejection of claims 1 through 4, 6, 11 through 18, and 21 through 24 under 35 U.S.C. § 112, first paragraph, be withdrawn.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,331,450 to Uemura

Claims 1 through 3, 6, 12, 14, 17, 21, 23 and 24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Uemura (U.S. Patent No. 6,331,450). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 recites the act of "forming a pattern of *mutually transverse channels* in said active surface to a depth below said at least one layer of integrated circuitry, *said channels circumscribing a semiconductor element location* comprised of at least one individual die." (Emphasis added.) Claim 1 also recites the act of "forming a layer of encapsulant material over substantially all of said active surface and into said channels such that a surface of said layer of encapsulant material *has a pattern of depressions over said channels.*" (Emphasis added.)

Uemura is directed to a method of forming a flip-chip type device from a plurality of flip-chip semiconductor device units integrated together on a common substrate. Fig. 1 illustrates a sectional view of a light-emitting device (LED) 100 used in the manufacturing process embodiments according to Uemura. LED 100 includes a recess (unnumbered) formed in the upper surface thereof, and a negative electrode 140 is disposed within the recess on a layer 103 of the LED circuitry (col. 4, lines 59-67). A positive electrode 120 is disposed adjacent to the recess on a layer 106 of the LED circuitry (col. 5, lines 1-4).

Figs. 2A-2F illustrate process steps according to a first embodiment for sealing multiple LED's 100 contained in a common substrate 10 with a sealing resin 230. Initially, a resist 210 is formed over substrate 10 with plating-film-growth parts 211 (col. 5, lines 47-54). Pillars or "plating films" 220 are formed in plating-film-growth parts 211 and resist 210 is removed leaving pillars 220 exposed (col. 5, lines 54-60). Next, LED's 100 are sealed with resin 230, which is deposited in a sufficient amount so that resin 230 is at substantially the same height as pillars 220 (col. 5, line 62 - col. 6, line 1). Solder bumps 240 are then formed on pillars 220, and LED's 100 are separated by dividing substrate 10 into distinct pieces (col. 6, lines 4-12). In a second embodiment illustrated by Figs. 3A-3D, the process steps are substantially the same, except resist 210 is left in place and is also used for resin 230 (col. 6, line 61 - col. 7, line 16).

Applicants respectfully submit that Uemura fails to describe every element of claim 1. Uemura does not describe the claim 1 limitation of "forming a pattern of *mutually transverse channels* in said active surface to a depth below said at least one layer of integrated circuitry, *said channels circumscribing a semiconductor element location* comprised of at least one individual die." (Emphasis added.) There is nothing in the disclosure of Uemura to indicate that the recesses in LED's 100 containing negative electrode 140 form mutually transverse channels, nor is there any indication that such recesses circumscribe a semiconductor element location comprised of at least one individual die. Likewise, Uemura does not describe the claim 1 limitation of "forming a layer of encapsulant material over substantially all of said active surface and into said channels such that a surface of said layer of encapsulant material *has a pattern of depressions over said channels.*" (Emphasis added.) In the first embodiment, Uemura merely discloses that resin 230 "is introduced onto the flip-chip-device units 100 in a sufficient amount so that the resin 230 is at substantially the same height as (and flush with the top ends of) the plating films 220" (col. 5, line 62 - col. 6, line 1). In the second embodiment, Uemura discloses that "resin 230 is uniformly applied to the substrate 10" (col. 6, lines 65-66), which contradicts the Office's assertion regarding the existence of depressions in the surface of resin 230.

Accordingly, claim 1 is allowable over Uemura under the provisions of 35 U.S.C. § 102(e). Claims 2 through 3, 6, 12, 14, 17, 21, 23 and 24, which depend from and incorporate all of the limitations of claim 1, are also allowable.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,331,450 to Uemura and further of U.S. Patent No. 4,610,079 to Abe et al.

Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Uemura (U.S. Patent No. 6,331,450) and further of Abe et al. (U.S. Patent No. 4,610,079). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
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> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 4 is improper because it fails to establish a *prima facie* case of obviousness.

Abe et al. is directed to a method of dicing a semiconductor wafer and is combined with Uemura to provide the teaching of V-shaped channels having sloped side walls. As previously discussed, claim 1 recites the limitation of "forming a layer of encapsulant material over substantially all of said active surface and into said channels *such that a surface of said layer of encapsulant material has a pattern of depressions over said channels*." (Emphasis added.) Neither Uemura nor Abe et al. teach or suggest this limitation.

Accordingly, claim 1 is allowable over the cited references, and claim 4, which depends from claim 1, is also allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Obviousness Rejection Based on U.S. Patent No. 6,331,450 to Uemura taken with U.S. Patent No. 6,181,569 to Chakravorty

Claims 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Uemura (U.S. Patent No. 6,331,450) taken with Chakravorty (U.S. Patent No. 6,181,569). Applicants respectfully traverse this rejection, as hereinafter set forth.

Chakravorty is directed to a method of fabricating chip size packages wherein a wafer 301 is encapsulated with a polymeric encapsulant layer 312 (col. 9, lines 55-59), and is combined with Uemura to provide the teaching of forming an intermediate conductive element from a solder ball or a wire bonding capillary. As previously discussed, Uemura fails to describe the claim 1 limitation of "forming a layer of encapsulant material over substantially all of said active surface and into said channels *such that a surface of said layer of encapsulant material has a pattern of depressions over said channels*." (Emphasis added.) Chakravorty also fails to teach or suggest forming a pattern of depressions over channels as recited in claim 1. In fact, Chakravorty expressly states that after encapsulation "the surface of wafer 301 is covered with the encapsulant, and thus the scribe lines are not visible." (col. 12, lines 25-27).

Accordingly, claim 1 is allowable over the cited references, and claims 11 and 13, which depend from claim 1, are also allowable.

Obviousness Rejection Based on U.S. Patent No. 6,331,450 to Uemura and further of U.S. Patent No. 5,933,713 to Farnworth

Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Uemura (U.S. Patent No. 6,331,450) and further of Farnworth (U.S. Patent No. 5,933,713). Applicants respectfully traverse this rejection, as hereinafter set forth.

The Farnworth '713 Patent is directed to a method of forming an overmolded chip scale package and is combined with Uemura to provide the teaching of specific encapsulant materials recited in claim 17. As previously discussed, claim 1 recites the limitation of "forming a layer of

encapsulant material over substantially all of said active surface and into said channels *such that a surface of said layer of encapsulant material has a pattern of depressions over said channels.*" (Emphasis added.) Neither Uemura nor the Farnworth '713 Patent teach or suggest this limitation.

Accordingly, claim 1 is allowable over the cited references, and claim 17, which depends from claim 1, is also allowable.

Obviousness Rejection Based on U.S. Patent No. 6,331,450 to Uemura and further of U.S. Patent No. 5,824,569 to Brooks et al.

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Uemura (U.S. Patent No. 6,331,450) and further of Brooks et al. (U.S. Patent No. 5,824,569). Applicants respectfully traverse this rejection, as hereinafter set forth.

Brooks et al. discloses a semiconductor device having ball bonded pads and is combined with Uemura to provide the teaching of forming an encapsulant material on the back of a semiconductor substrate. As previously discussed, claim 1 recites the limitation of "forming a layer of encapsulant material over substantially all of said active surface and into said channels *such that a surface of said layer of encapsulant material has a pattern of depressions over said channels.*" (Emphasis added.) Neither Uemura nor Brooks et al. teach or suggest this limitation.

Accordingly, claim 1 is allowable over the cited references, and claim 18, which depends from claim 1, is also allowable.

Obviousness Rejection Based on U.S. Patent No. 6,331,450 to Uemura and further of U.S. Patent No. 6,107,164 to Ohuchi

Claim 22 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Uemura (U.S. Patent No. 6,331,450) and further of Ohuchi (U.S. Patent No. 6,107,164). Applicants respectfully traverse this rejection, as hereinafter set forth.

Ohuchi is combined with Uemura to provide the teaching of a bond pads over an intermediate conductive element before electrical connection to a conductive bump. As previously discussed, Uemura fails to describe the claim 1 limitation of "forming a layer of

encapsulant material over substantially all of said active surface and into said channels *such that a surface of said layer of encapsulant material has a pattern of depressions over said channels.*" (Emphasis added.)

Ohuchi discloses a method of using grooves as alignment marks when dicing an encapsulated wafer. According to that method, a wafer 10 is cut between respective semiconductor elemental devices to define grooves 22 (col. 3, lines 9-13). Next, the surface of wafer 10 is sealed with a resin 23, which is polished to expose posts 4 (col. 3, lines 29-33). The back of wafer 10 is also polished to expose grooves 22 through the back of wafer 10 (col. 3, lines 36-42). Wafer 10 is then cut from the back side along grooves 22 to provide individual semiconductor devices (col. 3, lines 45-53). As such, the method disclosed by Ohuchi also does not teach or suggest forming a layer of encapsulant material having a pattern of depressions over channels formed in a semiconductor substrate.

Accordingly, claim 1 is allowable over the cited references, and claim 22, which depends from claim 1, is also allowable.

Obviousness Rejection Based on U.S. Patent No. 6,331,450 to Uemura and U.S. Patent No. 6,181,569 to Chakravorty, as applied to claims 11 and 13, and further of U.S. Patent No. 6,020,629 to Farnworth

Claims 12 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Uemura (U.S. Patent No. 6,331,450) and Chakravorty (U.S. Patent No. 6,181,569), as applied to claims 11 and 13, and further of Farnworth (U.S. Patent No. 6,020,629). Applicants respectfully traverse this rejection, as hereinafter set forth.

The Farnworth '629 Patent is combined with Uemura and Chakravorty to provide the teachings of forming pillars of conductor-filled epoxies or metal-filled elastomers as recited in claim 12 and 15. As previously discussed, claim 1 recites the limitation of "forming a layer of encapsulant material over substantially all of said active surface and into said channels *such that a surface of said layer of encapsulant material has a pattern of depressions over said channels.*" (Emphasis added.) None of Uemura, Chakravorty, or the Farnworth '629 Patent teach or suggest this limitation.

Accordingly, claim 1 is allowable over the cited references, and claims 12 and 15, which depend from claim 1, are also allowable.

Obviousness Rejection Based on U.S. Patent No. 6,331,450 to Uemura and further of U.S. Patent No. 6,137,164 to Yew et al.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Uemura (U.S. Patent No. 6,331,450) and further of Yew et al. (U.S. Patent No. 6,137,164). Applicants respectfully traverse this rejection, as hereinafter set forth.

Yew et al. discloses a stacked face-to-face integrated circuit packaging structure and is combined with Uemura to provide the teaching of forming an external conductive element from an anisotropically conductive film. As previously discussed, claim 1 recites the limitation of "forming a layer of encapsulant material over substantially all of said active surface and into said channels *such that a surface of said layer of encapsulant material has a pattern of depressions over said channels*." (Emphasis added.) Neither Uemura nor Yew et al. teach or suggest this limitation.

Accordingly, claim 1 is allowable over the cited references, and claim 16, which depends from claim 1, is also allowable.

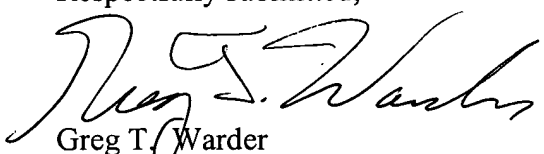
ENTRY OF AMENDMENTS

The proposed amendments to the specification and to claim 1 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1 through 4, 6, 11 through 18, and 21 through 24 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Applicants further note that claim 25 has been withdrawn from consideration as being drawn to a non-elected species. Applicants consider claim 1 to be generic, and note that claim 25 would be allowable upon allowance of claim 1. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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